UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,971	01/09/2001	Salman Akram	MI22-1572	7766

21567 7590 04/30/2002

WELLS ST. JOHN P.S.
601 W. FIRST
SUITE 1300
SPOKANE, WA 99201-3828

EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/756,971	AKRAM, SALMAN	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *68-74* is/are allowed.

6)☒ Claim(s) *42-57 & 63-67* is/are rejected.

7)☒ Claim(s) *58-62* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Objection of the Drawings as they refer to reference numbers 58b and 58c has been withdrawn. Applicant's response fully explains where in the specification these reference numbers are discussed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 42 is rejected under 35 U.S.C. 102(e) as being anticipated by Jiang et al., US Patent 6,048,755.

Jiang teaches a method of making a BGA package (Figure 6A) comprising:

providing an insulative substrate with circuitry thereon (56) and having an opening (64) therein;

adhering a die having circuitry (16) to the substrate (56) with an filled epoxy adhesive (72); and

electrically connecting the die (16) to the substrate (56) through the opening (64) using bonding wires (94).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 57 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakashima et al., US Patent 5,661,086.

Nakashima teaches a process of making a plurality of strip lead frame devices comprising:

forming a connected circuit substrates frame made of an glass fabrics reinforced epoxy resin (an insulative substrate) having a lead pattern on one face and an opening therein (6, 43-7, 4);

forming a connected metals frame and adhering it to said connected circuit substrates frame to the other face of the connected circuit substrates frame;

mounting a die onto the connected metals frame within the opening in the connected circuit substrates; and

electrically connecting using bond wires the die to the lead pattern on the connected circuit substrates wherein the bond wires extend through the opening (Figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al., US Patent 6,048,755, as applied to claim 42 above, and further in view of Chen et al., US Patent 6,215,180.

Regarding claim 43, though Jiang only teaches using a filled epoxy (6, 8+), it would have been obvious to one of ordinary skill in the art at the time of the invention to use a silver filled epoxy because it is a commonly known and conventionally used type of filled epoxy adhesive. The use of conventional materials to perform there known functions in a conventional process is obvious. In re Raner 134 USPQ 343 (CCPA 1962).

With respect to claim 44, Jiang fails to teach the use of a metal foil contacting at least a portion of the chip.

Chen teaches a heat dissipating structure for IC packages comprising a heat dissipating member (59) made of Al, Cu, Fe, Ni or alloys thereof formed into a thin plate

(4, 39+) directly attached to a chip on an insulative substrate (32, 42 & 52) (Figures 1-6, 7C, 7D and 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat dissipating member of Chen in the invention of Jiang because Chen teaches that the attachment of the heat dissipating member directly to the chip most effectively removes heat (1, 41+), this heat removal improves IC performance and reliability (1, 13+).

Claims 45, 49, 50, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al., US Patent 6,048,755, in view of Chen et al., US Patent 6,215,180.

Jiang teaches a method of making a BGA package (Figure 6A) comprising:

providing an insulative substrate with circuitry thereon (56) with an opening (64);

adhering a die having circuitry (16) to the substrate (56) with an filled epoxy adhesive (72); and

electrically connecting the die (16) to the substrate (56) through the opening (64) using bonding wires (94).

Jiang fails to teach the use of a metal foil contacting at least a portion of the chip.

Chen teaches a heat dissipating structure for IC packages comprising a heat dissipating member (59) made of Al, Cu, Fe, Ni or alloys thereof formed into a thin plate (4, 39+) directly attached to a chip on an insulative substrate (32, 42 & 52) (Figures 1-6, 7C, 7D and 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat dissipating member of Chen in the invention of Jiang because Chen teaches that the attachment of the heat dissipating member directly to the chip most effectively removes heat (1, 41+), this heat removal improves IC performance and reliability (1, 13+).

Regarding claim 49, Chen teaches in Figure 4 that it is known in the prior art to attach a heat dissipater (46) to only a portion of the exposed surface of the chip.

With respect to claim 50, Chen teaches in Figure 5 the attaching of a heat dissipater (46) to all of the exposed surface of the chip.

As to claim 55, Chen teaches a heat dissipating member made of Al, Cu, Fe, Ni or alloys thereof formed into a thin plate (4, 39+).

Regarding claim 56, Jiang teaches attaching the chip to the substrate using a filled epoxy (6, 8+).

Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al., US Patent 6,048,755, in view of Chen et al., US Patent 6,215,180, as applied to claim 45 above, and further in view of Tummala et al, Packaging Handbook-Semiconductor Packaging, Part II, 2nd Edition, , 1997, pp. 898-901.

Jiang and Chen fail to teach the use of welding, specifically laser welding, to attach the heat-dissipating member to the chip.

Tummala teaches the use of laser welding to attach metal lids or platings to packages (900, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the laser welding technique described in Tummala in the invention of Chen because Tummala teaches laser welding is attractive "because of its high speed, very limited heat input to sensitive areas, ability to handle unconventional seal geometries, and noncontact nature" (900, last paragraph).

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al., US Patent 6,048,755, in view of Chen et al., US Patent 6,215,180, as applied to claim 45 above, and further in view of Tummala et al, Packaging Handbook-Subsystem Packaging, Part III, 2nd Edition, 1997, pp. 223-234.

Jiang and Chen, which teaches attaching the heat dissipating member using any adhesive epoxy known in the art (4, 47+), fail to teach attaching the heat dissipater to the chip using an electrically conductive adhesive.

Tummala teaches the use of electrically conductive adhesives to adhere chips to substrates.

The actual choosing of an electrically conductive adhesive would have been obvious to one of ordinary skill in the art at the time of the invention because electrically conductive adhesives are commonly known and conventionally used to attach chips to substrates. They provide reliable connections that supply good electrical interconnections (p 229).

Claims 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al., US Patent 6,048,755, in view of Chen et al., US Patent 6,215,180, as applied to claim 45 above, and further in view of Wang et al., US Patent 6,255,140.

Regarding claims 51, Jiang and Chen fail to teach attaching the heat dissipater to the second surface and the sidewalls of the chip.

Wang teaches a flip chip chip scale package comprising attaching a reversed U-shaped heat slug (312) to the chip which contacts one surface of the chip and overhangs the sidewalls of the chip (Figure 3A & 3, 1+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat slug of Wang in the combined inventions of Jiang and Chen because Wang teaches the heat slug provides heat dissipation, protects the chip from cracking (abstract) and the heat dissipation effect of the heat slug should be improved because of the increased contact surface area of the heat slug to the chip.

With respect to claim 52, Jiang and Chen fail to teach attaching the heat dissipater to the second surface and the sidewalls of the chip wherein the heat dissipater physically contacts the sidewall of the chip.

Wang teaches a flip chip chip scale package comprising attaching a reversed U-shaped heat slug (312) to the chip which contacts one surface of the chip and overhangs the sidewalls of the chip, possibly in physical contact with the chip sidewalls (3, 24+). Wang's teaching that a space "may exist" between the heat slug and the chip also means that a space does not necessarily have to exist.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat slug of Wang in the invention of Jiang and Chen because Wang teaches the heat slug provides heat dissipation, protects the chip from cracking

(abstract) and the heat dissipation effect of the heat slug should be improved because of the increased contact surface area of the heat slug to the chip.

As to claim 53, Jiang and Chen fail to teach attaching the heat dissipater to the second surface and the sidewalls of the chip wherein the heat dissipater is spaced from the sidewall of the chip by a gap.

Wang teaches a flip chip chip scale package comprising attaching a reversed U-shaped heat slug (312) to the chip which contacts one surface of the chip and overhangs the sidewalls of the chip, wherein a space may exist between the heat slug and the chip (Figure 3A and 3, 26+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat slug of Wang in the invention of Jiang and Chen because Wang teaches the heat slug provides heat dissipation, protects the chip form cracking (abstract) and the heat dissipation effect of the heat slug should be improved because of the increased contact surface area of the heat slug to the chip.

Regarding claim 54, Jiang and Chen fail to teach attaching the heat dissipater to the second surface and the sidewalls of the chip wherein the heat dissipater is spaced from the sidewall of the chip by a gap that is filled in with an electrically conductive epoxy.

Wang teaches a flip chip chip scale package comprising attaching a reversed U-shaped heat slug (312) to the chip which contacts one surface of the chip and overhangs the sidewalls of the chip, wherein a space may exist between the heat slug and the chip that may be filled in with a conductive epoxy (Figure 3A and 3, 26+).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 63-67 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent Numbers 6,214,641, 5,998,865, 5,817,535 and 5,723,907. Although the conflicting claims are not identical, they are not patentably distinct from each other because the inventions claimed are similar. Both claim an insulative substrate having cavities therein with openings within the cavities, dice placed within the openings and electrically connected to the substrate through the openings and placing a metal layer over the exposed surface of the dice.

Allowable Subject Matter

As in the previous office action, claims 58-62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach forming a board on chip package comprising forming a metal foil on one side of an insulative substrate, attaching a chip to the metal foil, and then connecting the chip to the substrate using electrical interconnects extending through the opening, wherein the metal foil extends beyond the sides of the die and this extension is then wrapped around the die.

Claims 68-74 are allowed, as discussed in the previous office action.

The following is a statement of reasons for the indication of allowable subject matter: prior art could not be located that taught the forming the package as claimed and then joining the metal foil to the substrate and the dice and then singulating to form individual packages by cutting the substrate and the metal foil.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents 6,343,019 (Jiang et al), 6,271,586 (Shen), 6,198,162 (Corisis) and 5,998,860 (Chan et al.) all teach inventions similar to the one in claim 42.

Chaney et al., US Patent 5,985,697, teaches attaching a cooling device to a chip wherein the cooling device touches the sidewalls of the chip.

US Patents 6,107,683 and 6,300,165, both to Castro et al., teach inventions similar to claim 57.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-Th (7:30-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
April 25, 2002